Appendix 2

Clean Set of Claims

In the Claims:

1. A multi-layer electrode for an integrated circuit, comprising:

a conductive barrier layer;

a first conductive liner deposited over the conductive barrier layer;

a second conductive liner deposited over the first conductive liner; and

a conductive layer deposited over the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material.

2. The multi-layer electrode according to Claim 1 wherein the second conductive liner comprises a conductive oxide.

3. The multi-layer electrode according to Claim 2 wherein the second conductive liner is 20-50 Angstroms thick.

4. The multi-layer electrode according to Claim 3 wherein the conductive layer and the first conductive liner comprise Pt.

5. The multi-layer electrode according to Claim 4 wherein the first conductive liner is 200-500 Angstroms thick.

6. The multi-layer electrode according to Claim 5 wherein the conductive barrier layer comprises TaSiN.

7. The multi-layer electrode according to Claim 6 wherein the integrated circuit comprises a DRAM or an FRAM.

8. A multi-layer electrode for an integrated circuit, comprising:

a conductive barrier layer;

a first conductive liner deposited over the conductive barrier layer;

a second conductive liner deposited over the first conductive liner, the second conductive liner comprising a conductive oxide; and

a conductive layer deposited on the second conductive liner.

9. The multi-layer electrode according to Claim 8 wherein the second conductive liner is 20-50 Angstroms thick.

10. The multi-layer electrode according to Claim 8 wherein the conductive layer and the first conductive liner comprise Pt.

11. The multi-layer electrode according to Claim 8 wherein the first conductive liner is 200-500 Angstroms thick.

12. The multi-layer electrode according to Claim 8 wherein the conductive barrier layer comprises TaSiN.

13. The multi-layer electrode according to Claim 8 wherein the integrated circuit comprises a DRAM or an FRAM.

21. The multi-layer electrode according to Claim 1 wherein the second conductive liner comprises IrO_2 or RuO_2.

22. The multi-layer electrode according to Claim 8 wherein the second conductive liner comprises IrO_2 or RuO_2.

23. The multi-layer electrode according to Claim 1 wherein the conductive layer and the first conductive liner comprise Pt, Ir, Ru, Pd, or combinations thereof.

24. The multi-layer electrode according to Claim 8 wherein the conductive layer and the first conductive liner comprise Pt, Ir, Ru, Pd, or combinations thereof.